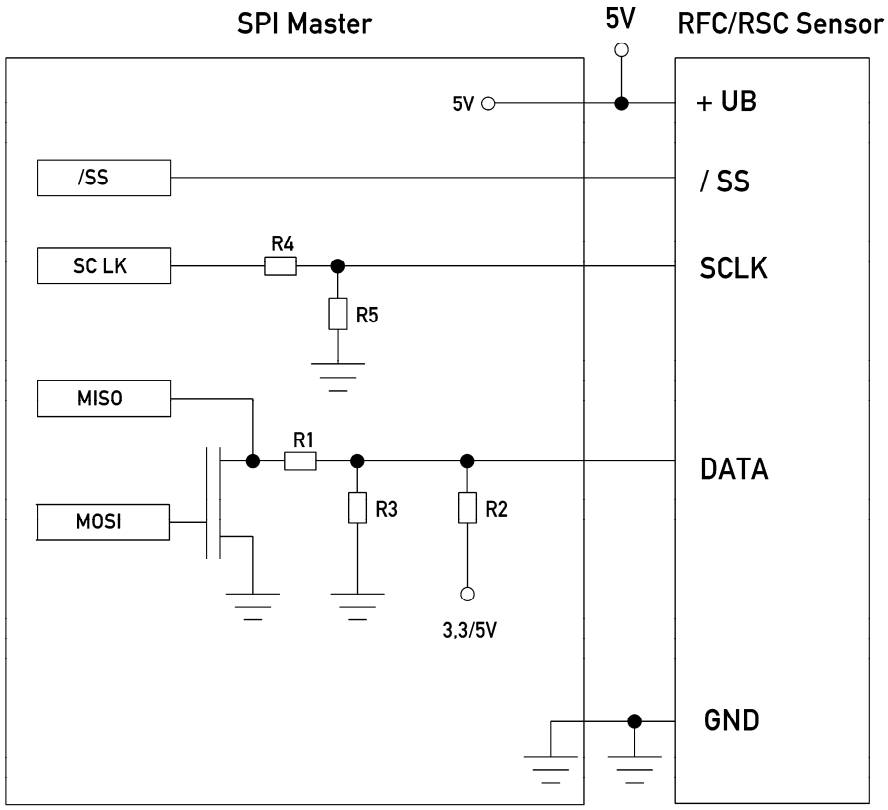
# Description SPI Serial Protocol for RSC/RFC digital

## 1 Electrical Characteristics

The serial protocol of the RSC/RFC is a three wires protocol
(/SS, SCLK, MOSI-MISO).
The RSC/RFC is considered as a slave mode:

- /SS pin is a 5V tolerant digital input
- SCLK pin is a 5V tolerant digital input
- MOSI-MISO pin is a 5V tolerant open drain digital input/output




| Application type | µCtrl supply (V) | Pull-up supply (V) | sensor supply (V) | R1 (Ω) | R2 (Ω) | R3 (kΩ) | R4 (Ω) | R5 (kΩ) | MOS type |
|---|---|---|---|---|---|---|---|---|---|
| 5VµCtrl w/o O.D. w/o 3.3V | 5V | 5V | 5V | 100 | 1000 | 20 | 1000 | 20 | BS 170 |
| 5VµCtrl w/o O.D. w 3.3V | 5V | 3,3V | 5V | 150 | 1000 | N/A | 1000 | 20 | BS 170 |
| 3,3VµCtrl w/o O.D. **(*1)** | 3,3V | 3,3V | 5V | 150 | 1000 | N/A | N/A | N/A | BS 170 |
| 5VµCtrl w O.D. w/o 3.3V**(*2)** | 5V | 5V | 5V | 100 | 1000 | 20 | 1000 | 20 | N/A |
| 3,3VµCtrl w O.D. | 3,3V | 3,3V | 5V | 150 | 1000 | N/A | N/A | N/A | N/A |

Table 3: Resistor values for common specific applications

*1 µCtrl w/ O.D.: Micro controller with open-drain capability (for example NEC V850 series)

*2 µCtrl w/o O.D.: Micro controller without open-drain capability (like TI TMS320 series or AMTEL AVR)

## 2 SPI Mode

CPHA = 1 even clock changes are used to sample the data
CPOL = 0 active high clock
The positive going edge shifts a bit to the slave´s output stage and the negative going edge samples the bit at the master´s input stage.

## 3 MOSI (Master OUT Slave IN)

The master sends a command to the slave to get the angle information.

## 4 MISO (Master In Slave Out)

The MISO of the slave is an open-collector stage. Due to the capacitive load a > 1k Ohm pull-up is used for the recessive high level (in fast and slow mode).

## 5 /SS Slave Select

The /SS pin enables a frame transfer (if CPHA = 1). It allows a re-synchronisation between Slave and Master in case of communication error.

## 6 Master Start-up

/SS, SCLK, MISO can be undefined during the Master start-up as long as the slave is re-synchronized before the first frame transfer.

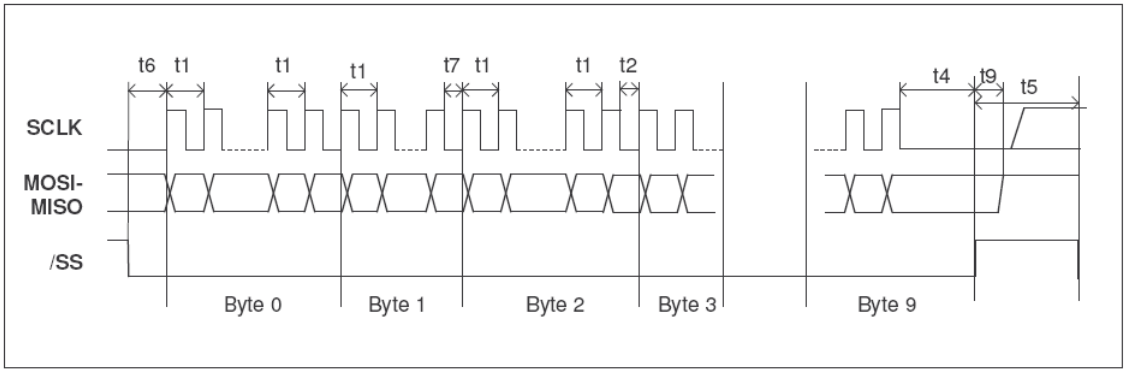
## 7 Slave Start-up

The slave start-up (after power-up, or an internal failure) takes 16ms. Within this time /SS and SCLK is ignored by the slave. The first frame can therefore be sent after 16ms.
MISO is high-impedant until the slave is selected by its /SS input.
RSC/RFC will cope with any signal from the master while starting up.

## 8 Timing

To synchronize communication, the master deactivates /SS high for at least t5 (1,5ms).
In this case, the slave will be ready to receive a new frame.

The master can re-synchronize at any time, even in the middle of a byte transfer.
Note: Any time shorter than t5 leads to an undefined frame state, because slave may or may not have seen /SS inactive.



| Timings | Min (15) | Max | Remarks |
|---|---|---|---|
| t1 | 2.3µs/6.9µs | - | No capacitve load on MISO. t1 is the minimum clock period for any bits within a byte |
| t2 | 12.5µs / 37.5µs | - | t2 is the minimum time between any other byte |
| t4 | 2.3µs / 6.9µs | - | Time between last clock and /SS=hi and= chip de selection |
| t5 | 300µs / 1500µs | - | Minimum /SS = Hi time where it is guaranteed that a frame recroniza-tions will be started. |
| t5 | 0µs | - | Minimum /SS = Hi time where it is guaranteed that NO frame recroniza-tions will be started. |
| t6 | 2.3µs/6.9µs | - | The time t6 defines the minimum time between /SS=Lo and the first clock edge. |
| t7 | 15µs/45µs | - | t7 is the minimum time between the start byte and byte 0 |
| t8 | 0µs | - | Minimum time where SS is deactivat-ed between a ID byte and a start byte |
| t9 | - | <1µs | Maximum time between /SS=Hi and MISO Bus High-Impedance |
| T start up | - | <10ms / 16ms | Minimum time between reset-inactive and any master signal change |

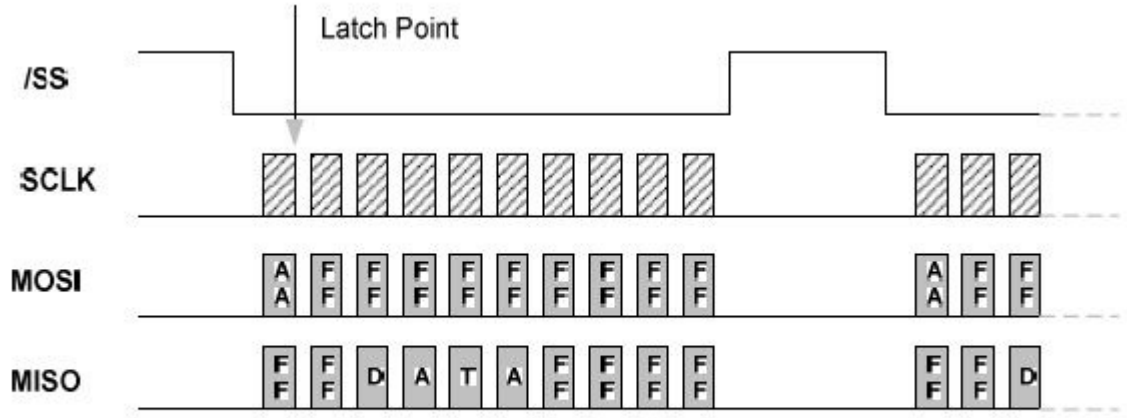
(15) Timings shown for oscillator base frequency of 20 MHz (fast mode) / 7 MHz (slow mode)

## 9 Slave Reset

On internal soft failures the slave will reset after 1 sec, or after an (error) frame is sent.
On internal hard failures the slave will reset itself. In that case the serial protocol will not come up. The serial protocol link is enable only after the completion of the first synchronisation (the master deactivates /SS for at least t5).

## 10 Frame Layer

Before each transmission of a data frame, the master should send a byte AAh to enable a frame transfer.
The latch point for the angle measurement is at the last clock of the first data frame byte.




Timing diagram - dual slave communication

## 11 Data Frame Structure

A data frame consists of 10 bytes

- 2 start bytes (AAh followed by FFh)
- 2 data bytes (Data 16 – most significant byte first)
- 2 inverted data bytes (/Data16 - most significant byte first)
- 4 all-high bytes

The Master should send AAh followed by nine bytes FFh.
The slave will answer with two bytes FFh followed by four data bytes and four bytes FFh.

## 12 Timing

There are no timing limits for frames: a frame transmission could be initiated at any time. There is no inter-frame time defined.

## 13 Data Structure

The Data16 could be a valid angle, or an error condition. The two meanings are distinguished by the LSB

Data 16: Angle A[13:0] with (Angle Span) /2^14

| Most Significant Byte | | | | | | | | Less Significant Byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB | MSB | | | | | | | LSB |
| A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 0 | 1 |

Data 16: Error

| Most Significant Byte | | | | | | | | Less Significant Byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB | MSB | | | | | | | LSB |
| E15 | E14 | E13 | E12 | E11 | E10 | E9 | E8 | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 |

| BIT | NAME | |
|---|---|---|
| E0 | 0 | |
| E1 | 1 | |
| E2 | F_ADCMONITOR | ADC Failure |
| E3 | F_ADCSATURA | ADC Saturation (Electrical failure or field too strong) |
| E4 | F_RGTOOLOW | Analog gain below trimmed threshold (likely reason: field too weak |
| E5 | F_MAGTOOLOW | Magnetic field too weak |
| E6 | F_MAGTOOHIGH | Magnetic field too strong |
| E7 | F_RGTOOHIGH | Analog gain above trimmed threshold (likely reason: field too strong |
| E8 | F_FGCLAMP | Never occuring in serial protocol |
| E9 | F_ROCLAMP | Analog chain rough offset compensation:clipping |
| E10 | F_MT7V | Device supply VDD greater than 7V |
| E11 | - | |
| E12 | - | |
| E13 | - | |
| E14 | F_DACMONITOR | Never occuring in serial protocol |
| E15 | - | |

## 14 Angle Calculation

All communication timing is independent (asynchronous) of the angle data processing.

The angle is calculated continuously by the slave:
- Slow Mode of RSC/RFC: every 1,5ms at most
- Fast Mode of RSC/RFC: every 350µs at most

The last angle calculated is hold to be read by the master at any time.
Note: Only valid angles are transferred by the slave, because any internal failure of the slave will lead to a soft reset.

## 15 Error Handling

In case of any errors listed in section 13, the serial protocol will be initialized and the error condition can be read by the master. The slave will perform a soft reset once the error frame is sent.

In case of any other errors (ROM CRC error, EEPROM CRC error, RAM check error, intelligent watchdog error,...) the slave´s serial protocol is not initialized. The MOSI/MISO pin will stay high impedant (no error frame is sent).